REMARKS

Reconsideration of the present application is respectfully requested.

Claims 1-26 previously presented for examination remain in the application. No

claims have been amended, canceled or added.

Claims 1-26 stand rejected under 35 U.S.C. § 103(a) as being considered

to be unpatentable over U.S. Patent No. 6,085,263 to Sharma et al. ("Sharma")

in view of U.S. Patent No. 6,718,454 to Ebner et al. ("Ebner").

Claim 1 includes the limitations

a prefetch engine to prefetch data from a distributed, coherent memory in
response to a first transaction from an input/output bus directed to the distributed,
coherent memory; and
an input/output coherent cache buffer to receive the prefetched data, the
coherent cache buffer being coherent with the distributed, coherent memory and
with other cache memories in a system including the input/output coherent cache
buffer,
the prefetch engine further to speculatively prefetch data in anticipation of
a need for the speculatively prefetched data in association with a second
input/output transaction if data has been prefetched for pending, memory-related
transactions from the input/output bus.

(Claim 1)(emphasis added).

As previously argued and as admitted in the present Office Action,

Sharma does not teach or suggest at least speculatively prefetching data as set

forth in claim 1. The combination of Ebner with Sharma, were such a

combination to be made, would also fail to teach or suggest the claimed features

of applicants' invention including at least the prefetch engine of claim 1 that

prefetches data and then speculatively prefetches data in anticipation of a need

for the data in association with an input/output transaction if data has been

prefetched for all pending transactions.

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As discussed previously, Sharma discloses a method and apparatus for employing commit-signals and prefetching to maintain inter-reference ordering in a high-performance I/O processor. (Sharma, Abstract).

Ebner discloses systems and methods for prefetch operations to reduce latency associated with memory access. According to Ebner, an I/O controller includes a fetch machine to provide or initiate retrieval of data stored at a requested address while a prefetch machine predicts future requests and keeps track of memory requests already initiated and queued. The I/O controller of Ebner also includes an arbiter to resolve memory accesses or data requests initiated by the fetch or prefetch machines. (Ebner, e.g. Abstract; Figure 4; col. 5, line 35 – col. 6, line 20; col 1, lines 55-68 and col. 2, lines 45-68).

The inclusion of an arbiter in Ebner and the accompanying description of its function indicate that the prefetch and fetch machines of Ebner operate concurrently such that prefetching can take place while fetching is in process.

In contrast, claim 1 sets forth a prefetch engine that is capable of speculatively prefetching if data associated with pending transactions has been prefetched, e.g. if the prefetch engine would otherwise be idle.

For at least this reason, Ebner cannot be considered to teach the prefetch engine of claim 1 and therefore, the combination of Sharma and Ebner would also fail to suggest the this claimed feature.

Independent claims 11 and 19 include a similar feature. Claims 2-10, claims 12-18 and claims 20-26 depend from and further limit claims 1, 11 and 19,
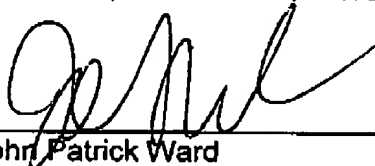
respectively and thus, should also be found to be patentably distinguished over Sharma and Ebner, alone or in combination.

Based on the foregoing, applicants respectfully submit that the applicable rejections and objections have been overcome and that claims 1-26 are in condition for allowance. If the examiner disagrees or believes that further discussion will expedite prosecution of this case, the examiner is invited to telephone applicants' representative Cynthia Thomas Faatz at (408) 765-2057.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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